Atty Docket No.: JCLA6831 Serial No.: 09/900,054

REMARKS

Claims 1-12 are presently pending, of which claims 1 and 7 have been amended for the purpose of clarification. No new matter has been added to the application by the amendments made to the claims, specification or otherwise in the application. For at least the following reasons it is submitted that this application is in condition for allowance. Reconsideration and withdrawal of the Examiner's rejections is respectfully requested.

Objection of claims:

Claim 1 was objected to because of informalities. Claim 1 has been amended according to Examiner's suggestion. Therefore, Applicant respectfully requests that the objection be withdrawn.

Rejection under 35 USC§103(a)

Claims 1-6 were rejected under 35 USC§103(a) as being unpatentable over Egawa et al. (U.S. Patent No. 6,376,278) in view of Belke, Jr. et al. (U.S. Patent 6,326,241) and Hung (U.S. Patent 6,380,624). According to Examiner, Egawa et al disclose the claimed invention

substantially as claimed except for specifically disclosing the chip having a plurality of bonding pads on each of which a gold bump is formed, and each package unit having a plurality of contact pads respectively connected to the corresponding bumps. However, Examiner has relied on Belke for the bonding pads and the package units. This rejection has carefully been considered but respectfully traversed.

Applicant wishes to direct the Examiner's attention to the basic requirements of a prima facie case of obviousness as set forth in the MPEP §2143. The section recites three basic requirements for establishing a prima facie case of obviousness. First, there must be some suggestion or motivation to combine the references. Second, there must be reasonable expectations of success. Third, the references must teach or suggest all the claim limitations.

Claim 1, as amended here, recites a flip chip packaging process comprising:

> *providing a wafer having a plurality of chips formed thereon, wherein each chip has an active surface provided with a plurality of bonding pads;*
>
> *forming a bump on each bonding pad;*
>
> *providing a plurality of individual substrates, wherein each substrate includes at least a package unit, each package unit having a plurality of contact pads thereon;*
>
> *respectively mounting the substrates onto the wafer such that each package unit corresponds to each chip and the contact pads are respectively connected to the corresponding bumps, wherein two neighboring substrates are separated by a gap;*
>
> *filling an underfill material between the substrates and the wafer, wherein the underfill material is introduced through the gaps between the substrates and from the*

boundary of the wafer;

solidifying the underfill material; and

dicing the wafer and the substrates to form a plurality of individualized packages, each individualized package including one chip and one package unit.

7. (once amended) A flip chip packaging process comprising:

providing a wafer having a plurality of chips formed thereon, wherein each chip has an active surface provided with a plurality of bonding pads;

providing a plurality of individual substrates, wherein each substrate includes at least a package unit, the package unit having a plurality of contact pads thereon;

forming a bump on each contact pad;

respectively mounting the substrates onto the wafer such that each package unit corresponds to one chip and the bonding pads are respectively connected to the corresponding bumps, wherein two neighboring substrates are separated by a gap;

filling an underfill material between the substrates and the wafer, wherein the underfill material is introduced through the gaps between the substrates and from the boundary of the wafer;

solidifying the underfill material; and

dicing the wafer and the substrates to form a plurality of individualized packages, each individualized package including one package unit and one chip.

Egawa et al, Belke and Hung fail to teach or suggest that *mounting a plurality of individual substrates onto the wafer which includes a plurality of the chips, filling an underfill material through the gaps between the substrates, and then dicing the wafer and the substrate.* In Egawa et al, the wafer 10 is mounted to the wiring substrate 62 through the bumps 22, the resin 34 subsequently seals the space between the wafer 10 and the wiring substrate 62, and then

the whole structure is diced into a plurality of preliminary structures 44. It is noted that the wiring substrate 62 mounted onto the wafer 10 is a continuous piece until the whole structure including the wafer 10 and the wiring substrate 62 is diced. Unlike Egawa et al, the claimed invention respectively mounts a plurality of individual substrates onto the wafer in a manner that two neighboring substrates are separated by a gap. The underfill material is filled between the substrates and the wafer through the gaps. The gap advantageously helps the subsequent step of filling the underfill material between the substrates and the wafer.

Furthermore, Examiner misconstrued the gap recited in the claimed invention as the gap 68 of Egawa et al. Applicant respectfully submits that the gap recited in the claimed invention significantly different from the gap 68. The gap in the claimed invention refers to the distance between the two adjacent substrates on the wafer before dicing process. Through the gap between the neighboring substrates, the underfill material will be filled better for the wafer level packaging. However, the gap 68 of Egawa et al refers to the removed portion after the whole structure is diced into a plurality of preliminary structures 44. Egawa's gap 68 does not help the underfilling at all.

It is well known in the art that underfilling between the substrate and the chip (wafer) is

critical to the flip chip packaging technology, because it is difficult to perfectly fill up the space between the substrate and the chip(wafer). Therefore, in the art, the wafer is usually divided into a plurality of chips before mounting the substrate. However, the wafer level packaging has been increasingly popular as its high productivity. Applicant has overcome the prior problems by mounting the individual substrates onto the wafer wherein the neighboring substrates is separated by a gap, subsequently underfilling through the gaps and then dicing the wafer and the substrates into a plurality of packages.

In view of the foregoing, even if those skilled in the art combine the teachings of Belke Jr. et al and Hung with the method of Egawa et al, still the combination can not react at the claimed invention. Applicant submits that amended claims 1 and 7 patentably distinguish over the prior art. Applicant respectfully submits that claims 2-6 and 8-12, respectively dependent upon claims 1 and 7, patentably distinguish over prior art for at least the reasons set forth above with respect to claims 1 and 7. Withdrawal of this rejection under 35 USC§103(a) is respectfully requested.

CONCLUSION

In view of the foregoing, Applicant respectfully requests reconsideration and reexamination of claims 1-12, and submits that these claims are in condition for allowance. In the event a telephone conversation would expedite the prosecution of this application, the Examiner is encouraged to contact the undersigned attorney to discuss the application.

Respectfully submitted,
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Version with markings to show changes made

In The Claims:

Claims 1 and 7 have been amended as follows:

1. (Once Amended) A flip chip packaging process comprising:

providing a wafer having a plurality of chips formed thereon, wherein each chip has an active surface provided with a plurality of bonding pads;

forming a bump on each bonding pad;

providing a plurality of individual substrates, wherein each substrate includes at least a package unit, each package unit having a plurality of contact pads thereon;

respectively mounting the substrates onto the wafer such that each package unit corresponds to each chip and the contact pads are respectively connected to the corresponding bumps, wherein two neighboring substrates are separated by a gap;

filling an underfill material between the substrates and the wafer, wherein the underfill material [being]is introduced through the gaps between the substrates and from the boundary of the wafer;

solidifying the underfill material; and

dicing the wafer and the substrates to form a plurality of individualized packages, each individualized package including one chip and one package unit.

7. (Once Amended) A flip chip packaging process comprising:

providing a wafer having a plurality of chips formed thereon, wherein each chip has an

active surface provided with a plurality of bonding pads;

providing a plurality of individual substrates, wherein each substrate includes at least a package unit, the package unit having a plurality of contact pads thereon;

forming a bump on each contact pad;

respectively mounting the substrates onto the wafer such that each package unit corresponds to one chip and the bonding pads are respectively connected to the corresponding bumps, wherein two neighboring substrates are separated by a gap;

filling an underfill material between the substrates and the wafer, wherein the underfill material is introduced through the gaps between the substrates and from the boundary of the wafer;

solidifying the underfill material; and

dicing the wafer and the substrates to form a plurality of individualized packages, each individualized package including one package unit and one chip.